Research Article

Optimization and Implementation of Scaling-Free CORDIC-Based Direct Digital Frequency Synthesizer for Body Care Area Network Systems

Ying-Shen Juang,[1] Lu-Ting Ko,[2] Jwu-E. Chen,[2] Tze-Yun Sung,[3] and Hsi-Chin Hsin[4]

[1] *Department of Business Administration, Chung Hua University, Hsinchu City 300-12, Taiwan*
[2] *Department of Electrical Engineering, National Central University, Chungli City 320-01, Taiwan*
[3] *Department of Microelectronics Engineering, Chung Hua University, Hsinchu City 300-12, Taiwan*
[4] *Department of Computer Science and Information Engineering, National United University, Miaoli 360-03, Taiwan*

Correspondence should be addressed to Tze-Yun Sung, bobsung@chu.edu.tw

Coordinate rotation digital computer (CORDIC) is an efficient algorithm for computations of trigonometric functions. Scaling-free-CORDIC is one of the famous CORDIC implementations with advantages of speed and area. In this paper, a novel direct digital frequency synthesizer (DDFS) based on scaling-free CORDIC is presented. The proposed multiplier-less architecture with small ROM and pipeline data path has advantages of high data rate, high precision, high performance, and less hardware cost. The design procedure with performance and hardware analysis for optimization has also been given. It is verified by Matlab simulations and then implemented with field programmable gate array (FPGA) by Verilog. The spurious-free dynamic range (SFDR) is over 86.85 dBc, and the signal-to-noise ratio (SNR) is more than 81.12 dB. The scaling-free CORDIC-based architecture is suitable for VLSI implementations for the DDFS applications in terms of hardware cost, power consumption, SNR, and SFDR. The proposed DDFS is very suitable for medical instruments and body care area network systems.

1. Introduction

Direct digital frequency synthesizer (DDFS) has been widely used in the modern communication systems. DDFS is preferable to the classical phase-locked-loop- (PLL-) based synthesizer in terms of switching speed, frequency resolution, and phase noise, which are beneficial to the high-performance communication systems. Figure 1 depicts the conventional DDFS architecture [1], which consists of a phase accumulator, a sine/cosine generator, a digital-to-analog converter (DAC), and a low-pass filter (LPF). As noted, two inputs: the reference clock and the frequency control word (FCW) are used; the phase accumulator integrates FCW to produce an angle in the interval of $[0, 2\pi)$, and the sine/cosine generator computes the sinusoidal values. In practice, the sine/cosine generator is implemented digitally, and thus followed by digital-to-analog conversion and low-pass filtering for analogue

outputs. Such systems can be applied in many fields, especially in industrial, biological, and medical applications [2–4].

The simplest way to implement the sine/cosine generator is to use ROM lookup table (LUT). However, a large ROM is needed [5]. Several efficient compression techniques have been proposed to reduce the lookup table size [5–10]. The quadrant compression technique can compress the lookup table and then reduce the ROM size by 75% [6]. The Sunderland architecture splits the ROM into two smaller memories [7], and the Nicholas architecture improves the Sunderland architecture to achieve a higher ROM-compression ratio $(32 : 1)$ [8]. The ROM size can be further reduced by using the polynomial approximations [11–18] or CORDIC algorithm [19–27]. In the polynomial approximations-based DDFSs, the interval of $[0, \pi/4]$ is divided into subintervals, and sine/cosine functions are evaluated in each subinterval.
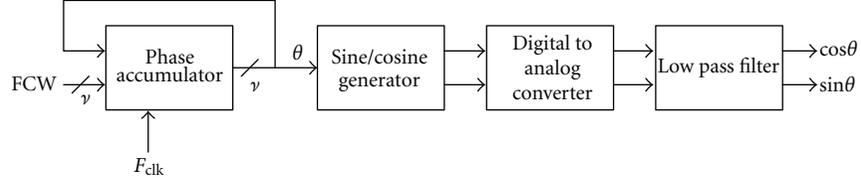
FIGURE 1: The conventional DDFS architecture.

The polynomial approximations-based DDFS requires a ROM to store the coefficients of the polynomials and the polynomial evaluation hardware with multipliers. In the circular mode of CORDIC, which is an iterative algorithm to compute sine/cosine functions, an initial vector is rotated with a predetermined sequence of subangles such that the summation of the rotations approaches the desired angle [28, 29]. CORDIC has been widely used for the sine/cosine generator of DDFS [19–27]. Compared to the lookup table-based DDFS, the CORDIC-based DDFS has the advantage of avoiding the exponential growth of hardware complexity while the output word size increases [30–33].

In Figure 1, the word length of the phase accumulator is v bits; thus, the period of the output signal is as follows:

$$T_o = \frac{2^v T_s}{\text{FCW}}, \tag{1}$$

where FCW is the phase increment and T_s denotes the sampling period. It is noted that the output frequency can be written by

$$F_o = \frac{1}{T_0} = \frac{F_s}{2^v} \cdot \text{FCW}. \tag{2}$$

According to the equation above, the minimum change of output frequency is given by

$$\Delta F_{o,\text{min}} = \frac{F_s}{2^v}(\text{FCW} + 1) - \frac{F_s}{2^v}\text{FCW} = \frac{F_s}{2^v}. \tag{3}$$

Thus, the frequency resolution of DDFS is dependent on the word length of the phase accumulator as follows:

$$\Delta F_o \geq \frac{F_s}{2^v}. \tag{4}$$

The bandwidth of DDFS is defined as the difference between the highest and the lowest output frequencies. The highest frequency is determined by either the maximum clock rate or the speed of logic circuitries; the lowest frequency is dependent on FCW. Spurious-free dynamic range (SFDR) is defined as the ratio of the amplitude of the desired frequency component to that of the largest undesired one at the output of DDFS, which is often represented in dB$_c$ as follows:

$$\text{SFDR} = 20 \log\left(\frac{A_p}{A_s}\right) = 20 \log\left(A_p\right) - 20 \log(A_s), \tag{5}$$

where A_p is the amplitude of the desired frequency component and A_s is the amplitude of the largest undesired one.

In this paper, a novel DDFS architecture based on the scaling-free CORDIC algorithm [34] with ROM mapping is presented. The rest of the paper is organized as follows. In Section 2, CORDIC is reviewed briefly. In Section 3, the proposed DDFS architecture is presented. In Section 4, the hardware implementation of DDFS is given. Conclusion can be found in Section 5.

2. The CORDIC Algorithm

CORDIC is an efficient algorithm that evaluates various elementary functions including sine and cosine functions. As hardware implementation might only require simple adders and shifters, CORDIC has been widely used in the high speed applications.

2.1. The CORDIC Algorithm in the Circular Coordinate System.
A rotation of angle θ in the circular coordinate system can be obtained by performing a sequence of micro-rotations in the iterative manner. Specifically, a vector can be successively rotated by the use of a sequence of pre-determined step-angles: $\alpha(i) = \tan^{-1}(2^{-i})$. This methodology can be applied to generate various elementary functions, in which only simple adders and shifters are required. The conventional CORDIC algorithm in the circular coordinate system is as follows [28, 29]:

$$x(i + 1) = x(i) - \sigma(i)2^{-i}y(i), \tag{6}$$

$$y(i + 1) = y(i) + \sigma(i)2^{-j}x(i), \tag{7}$$

$$z(i + 1) = z(i) - \sigma(i)\alpha(i), \tag{8}$$

$$\alpha(i) = \tan^{-1}2^{-i}, \tag{9}$$

where $\sigma(i) \in \{-1, +1\}$ denotes the direction of the ith micro-rotation, $\sigma_i = \text{sign}(z(i))$ with $z(i) \to 0$ in the vector rotation mode [34], $\sigma_i = -\text{sign}(x(i)) \cdot \text{sign}(y(i))$ with $y(i) \to 0$ in the angle accumulated mode [34], the corresponding scale factor $k(i)$ is equal to $\sqrt{1 + \sigma^2(i)2^{-2i}}$, and $i = 0, 1, \ldots, n - 1$. The product of the scale factors after n micro-rotations is given by

$$K_1 = \prod_{i=0}^{n-1} k(i) = \prod_{i=0}^{n-1} \sqrt{1 + 2^{-2i}}. \tag{10}$$

In the vector rotation mode, $\sin \theta$ and $\cos \theta$ can be obtained with the initial value: $(x(0), y(0)) = (1/K_1, 0)$. More

specifically, x_{out} and y_{out} are computed from the initial value: $(x_{\text{in}}, y_{\text{in}}) = (x(0), y(0))$ as follows:

$$\begin{bmatrix} x_{\text{out}} \\ y_{\text{out}} \end{bmatrix} = K_1 \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_{\text{in}} \\ y_{\text{in}} \end{bmatrix}. \tag{11}$$

2.2. Scaling-Free CORDIC Algorithm in the Circular Coordinate System. Based on the following approximations of sine and cosine functions:

$$\sin\alpha(i) \cong \alpha(i) = 2^{-i},$$

$$\cos\alpha(i) \cong 1 - \frac{\alpha^2(i)}{2} = 1 - 2^{-(2i+1)}, \tag{12}$$

the scaling-free CORDIC algorithm is thus obtained by using (6), (7), and the above. In which, the iterative rotation is as follows:

$$\begin{bmatrix} x(i+1) \\ y(i+1) \end{bmatrix} = \begin{bmatrix} 1 - 2^{-(2i+1)} & 2^{-i} \\ -2^{-i} & 1 - 2^{-(2i+1)} \end{bmatrix} \begin{bmatrix} x(i) \\ y(i) \end{bmatrix},$$

$$z(i+1) = z(i) - 2^{-i}. \tag{13}$$

For the word length of w bits, it is noted that the implementation of scaling-free CORDIC algorithm utilizes four shifters and four adders for each micro-rotation in the first $w/2$-microrotations; it reduces two shifters and two adders for each microrotation in the last $w/2$-micro-rotations [24, 34, 35].

3. Design and Optimization of the Scaling-Free CORDIC-Based DDFS Architecture

In this section, the architecture together with performance analysis of the proposed DDFS is presented. It is a combination of the scaling-free-CORDIC algorithm and LUT; this hybrid approach takes advantage of both CORDIC and LUT to achieve high precision and high data rate, respectively. The proposed DDFS architecture consists of phase accumulator, radian converter, sine/cosine generator, and output stage.

3.1. Phase Accumulator. Figure 2 shows the phase accumulator, which consists of a 32-bit adder to accumulate the phase angle by FCW recursively. At time n, the output of phase accumulator is $\phi = (n \cdot \text{FCW})/2^{32}$ and the sine/cosine generator produces $\sin((n \cdot \text{FCW})/2^{32})$ and $\cos((n \cdot \text{FCW})/2^{32})$. The *load* control signal is used for FCW to be loaded into the register, and the *reset* signal is to initialize the content of the phase accumulator to zero.

3.2. Radian Converter. In order to convert the output of the phase accumulator into its binary representation in radians, the following strategy has been adopted. Specifically, an efficient ROM reduction scheme based on the symmetry property of sinusoidal wave can be obtained by simple logic operations to reconstruct the sinusoidal wave from its first quadrant part only. In which, the first two MSBs of an angle
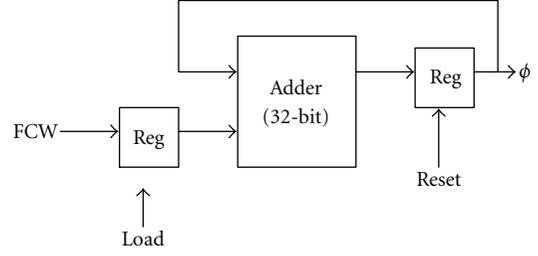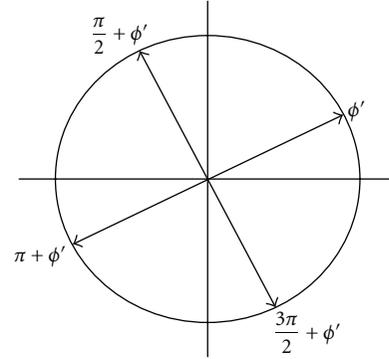

FIGURE 2: The phase accumulator in DDFS.

FIGURE 3: Symmetry-based map of an angle in either the second, third, or fourth quadrant to the corresponding angle in the first quadrant.

indicate the quadrant of the angle in the circular coordinate and the third MSB indicates the half portion of the quadrant; thus, the first three MSBs of an angle are used to control the interchange/negation operation in the output stage. As shown in Figure 3, the corresponding angles of ϕ' in the second, third, and fourth quadrants can be mapped into the first quadrant by setting the first two MSBs to zero. The radian of ϕ' is therefore obtained by $\theta = (\pi/4)\phi'$, which can be implemented by using simple shifters and adders array shown in Figure 4. Note that the third MSB of any radian value in the upper half of a quadrant is 1, and the sine/cosine of an angle γ in the upper half of a quadrant can be obtained from the corresponding angle in the lower half as shown in Figure 5. More specifically, as $\cos\gamma = \sin((\pi/2) - \gamma)$ and $\sin\gamma = \cos((\pi/2) - \gamma)$, the normalized angle can be obtained by replacing θ with $\theta' = 0.5 - \theta$ while the third MSB is 1. In case the third MSB is 0, there is no need to perform the replacement as $\theta' = \theta$.

3.3. Sine/Cosine Generator. As the core of the DDFS architecture, the sine/cosine generator produces sinusoidal waves based on the output of the radian converter. Without loss of generality, let the output resolution be of 16 bits, for the sine/cosine generator consisting of a cascade of w processors, each of which performs the sub-rotation by a fixed angle of 2^{-i} radian as follows:

$$x(i+1) = \left(1 - \sigma(i)2^{-(2i+1)}\right)x(i) + \sigma(i)2^{-i}y(i),$$

$$y(i+1) = \left(1 - \sigma(i)2^{-(2i+1)}\right)y(i) - \sigma(i)2^{-i}x(i). \tag{14}$$

TABLE 1: The hardware costs in 16-bit DDFS with respect to the number of the replaced CORDIC stages (m: the number of the replaced CORDIC stages, 16-bit adder: 200 gates, 16-bit shift: 90 gates, and 1-bit ROM: 1 gate).

m	0	1	2	3	4	5	6	7
CORDIC processor requirement:								
CORDIC processor-A	7	5	4	3	2	1	0	0
CORDIC processor-B	9	9	9	9	9	9	9	8
Hardware cost:								
16-bit Adders	46	38	34	30	26	22	18	16
16-bit Shifters	46	38	34	30	26	22	18	16
ROM size (bits)	4×16	8×16	14×16	26×16	50×16	102×16	194×16	386×16
Total gate counts	13404	11148	10084	9116	8340	8012	8324	10816

TABLE 2: Control signals of the output stage.

MSB's of ϕ	ϕ	$xinv$	$yinv$	$swap$	$\cos 2\pi\phi$	$\sin 2\pi\phi$
0 0 0	$0 < 2\pi\phi < \dfrac{\pi}{4}$	0	0	0	$\cos\theta$	$\sin\theta$
0 0 1	$\dfrac{\pi}{4} < 2\pi\phi < \dfrac{\pi}{2}$	0	0	1	$\sin\theta$	$\cos\theta$
0 1 0	$\dfrac{\pi}{2} < 2\pi\phi < \dfrac{3\pi}{4}$	0	1	1	$-\sin\theta$	$\cos\theta$
0 1 1	$\dfrac{3\pi}{4} < 2\pi\phi < \pi$	1	0	0	$-\cos\theta$	$\sin\theta$
1 0 0	$-\pi < 2\pi\phi < -\dfrac{3\pi}{4}$	1	1	0	$-\cos\theta$	$-\sin\theta$
1 0 1	$-\dfrac{3\pi}{4} < 2\pi\phi < -\dfrac{\pi}{2}$	1	1	1	$-\sin\theta$	$-\cos\theta$
1 1 0	$-\dfrac{\pi}{2} < 2\pi\phi < -\dfrac{\pi}{4}$	1	0	1	$\sin\theta$	$-\cos\theta$
1 1 1	$-\dfrac{\pi}{4} < 2\pi\phi < 0$	0	1	0	$\cos\theta$	$-\sin\theta$

TABLE 3: Comparisons of the proposed DDFS with other related works.

DDFS	Kang and Swartzlander, 2006 [23]	Sharma et al., 2009 [26]	Jafari et al., 2005 [17]	Ashrafi and Adhami, 2007 [18]	Yi et al., 2006 [6]	De Caro et al., 2009 [27]	This work, Juang et al., 2012
Process (μm)	0.13	—	0.5	0.35	0.35	0.25	0.18
Core area (mm^2)	0.35	—	—	—	—	0.51	0.204
Maximum sampling rate (MHz)	1018	230	106	210	100	385	500
Power consumption (mW)	0.343	—	—	112	0.81	0.4	0.302
SFDR (dB$_c$)	90	54	—	72.2	80	90	86.85
SNR (dB)	—	—	—	67	—	70	81.12
Output resolution (bit)	17	10	14	12	16	13	16
Tuning latency (clock)	—	—	33	—	—	—	11

For $8 \leq i < 16$

$$x(i+1) = x(i) + \sigma(i)2^{-i}y(i),$$
$$y(i+1) = y(i) - \sigma(i)2^{-i}x(i),$$

(15)

where $\sigma(i) \in \{1, 0\}$ representing the positive or zero subrotation, respectively. Figure 6 depicts the CORDIC processor-A for the first 7 microrotations, which consists of four 16-bit

adders and four 16-bit shifters. The CORDIC processor-B with two 16-bit adders and two 16-bit shifters for the last 9 microrotations is shown in Figure 7.

The first m CORDIC stages can be replaced by simple LUT to reduce the data path at the cost of hardware complexity increasing exponentially. Table 1 depicts the hardware costs in 16-bit DDFS with respect to the number of the replaced CORDIC-stages, where each 16-bit adder, 16-bit
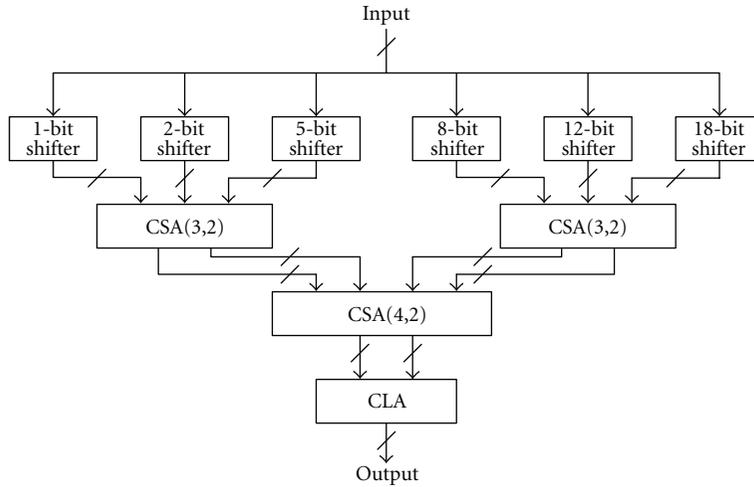
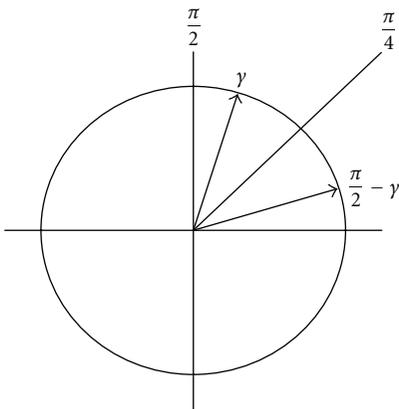FIGURE 4: The constant $(\pi/4)$ multiplier.

FIGURE 5: $\pi/4$-mirror map of an angle γ above $\pi/4$ to the corresponding angle $\pi/2 - \gamma$ below $\pi/4$.
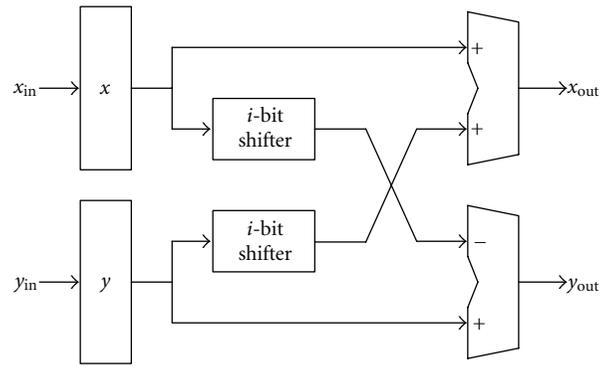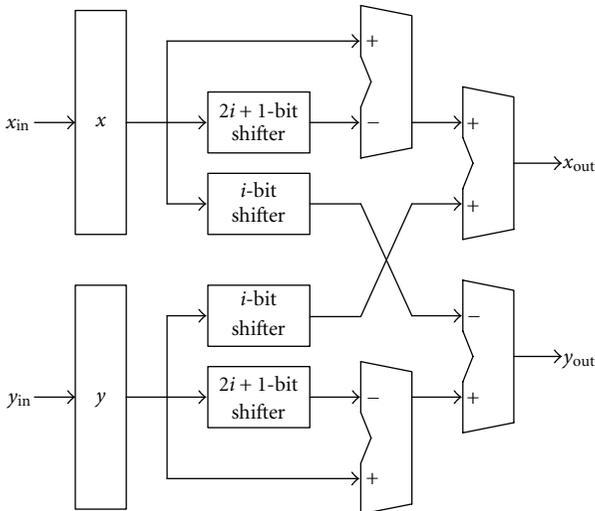

FIGURE 7: The CORDIC processor-B.

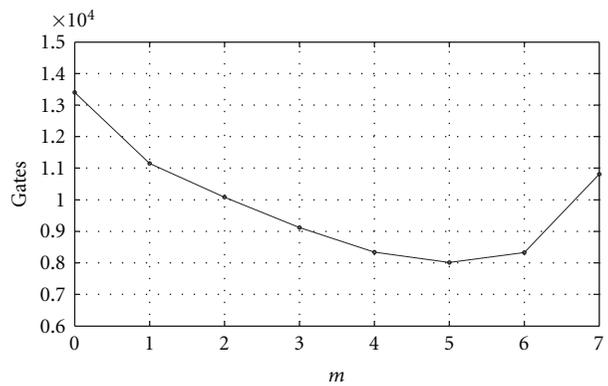FIGURE 6: The CORDIC processor-A.

FIGURE 8: Hardware requirements with respect to the replaced CORDIC stages.

shifter, and 1-bit memory require 200 gates, 90 gates, and 1 gate [36], respectively. Figure 8 shows the hardware requirements with respect to the number of the replaced CORDIC-stages [24]. Figure 9 shows the SFDR/SNRs with respect to
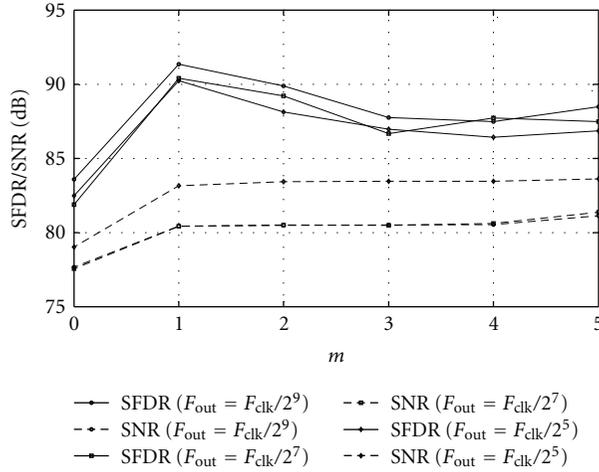
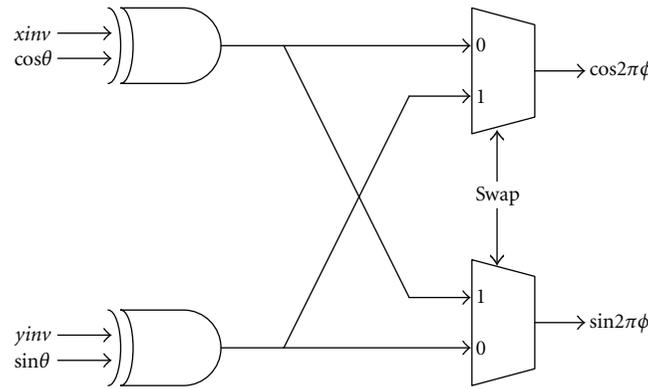Figure 9: SFDR/SNRs with respect to the replaced CORDIC-stages.
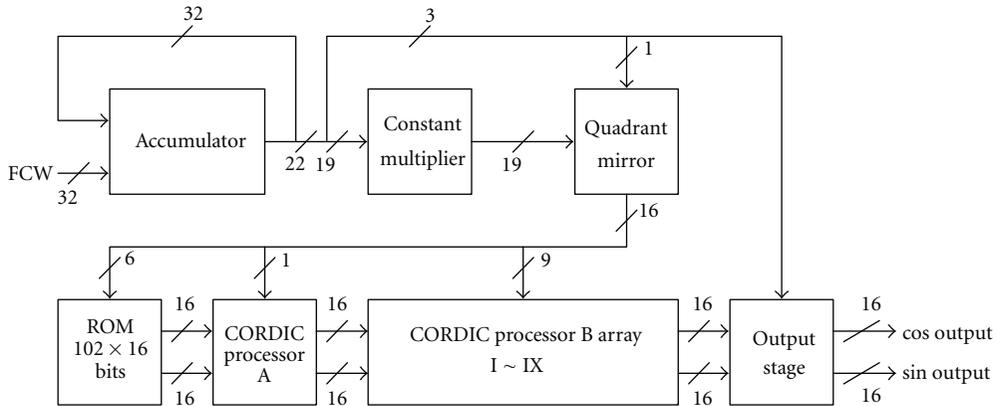

Figure 10: The output stage.

Figure 11: The proposed DDFS architecture.

the replaced CORDIC-stages [25]. As one can expect, based on the above figures, there is a tradeoff between hardware complexity and performance in the design of DDFS.

3.4. Output Stage. Figure 10 shows the architecture of output stage, which maps the computed $\sin\theta$ and $\cos\theta$ to the desired $\sin\phi$ and $\cos\phi$. As mentioned previously, the above mapping can be accomplished by simple negation and/or interchange operations. The three control signals: *xinv*, *yinv*, and *swap* derived from the first three MSBs of ϕ are shown in Table 2. *xinv* and *yinv* are for the negation operation of the output and *swap* for the interchange operation.
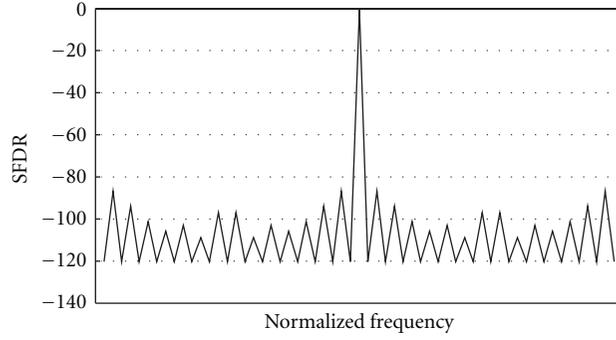
FIGURE 12: SFDR of the proposed DDFS architecture at output frequency $F_{clk}/2^5$.
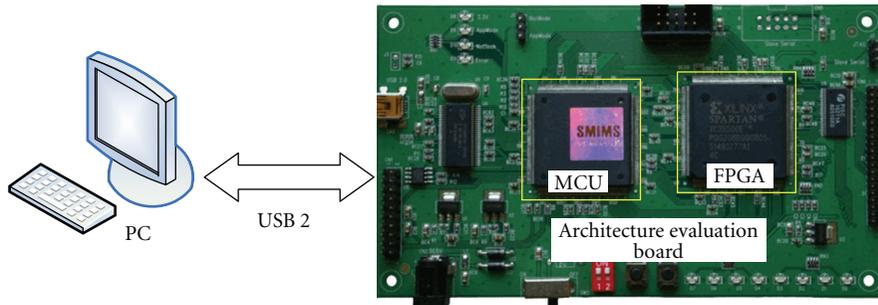

FIGURE 13: Block diagram and circuit board of the architecture development and verification platform.
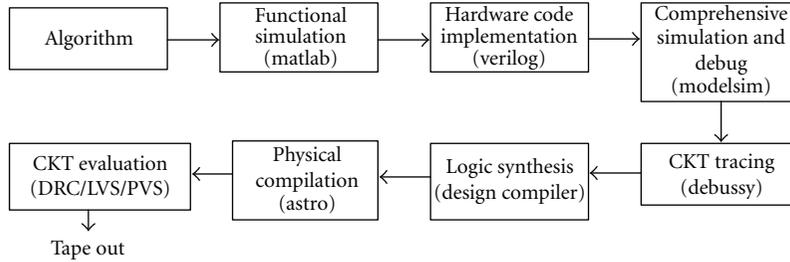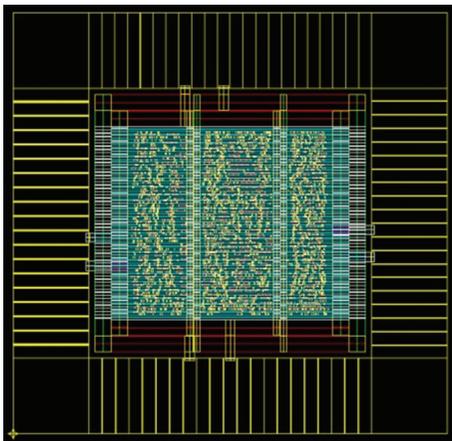

FIGURE 14: Cell-based design flow.

FIGURE 15: Layout view of the proposed scaling-free-CORDIC-based DDFS.

4. Hardware Implementation of the Scaling-Free CORDIC-Based DDFS

In this section, the proposed low-power and high-performance DDFS architecture ($m = 5$) is presented. Figure 11 depicts the system block diagram; SFDR of the proposed DDFS architecture at output frequency $F_{clk}/2^5$ is shown in Figure 12. As one can see, the SFDR of the proposed architecture is more than 86.85 dBc.

The platform for architecture development and verification has also been designed as well as implemented to evaluate the development cost [37–40]. The proposed DDFS architecture has been implemented on the Xilinx FPGA emulation board [41]. The Xilinx Spartan-3 FPGA has been integrated with the microcontroller (MCU) and I/O interface circuit (USB 2.0) to form the architecture development and verification platform.

Figure 13 depicts block diagram and circuit board of the architecture development and evaluation platform. In which, the microcontroller read data and commands from PC and writes the results back to PC via USB 2.0 bus; the Xilinx Spartan-3 FPGA implements the proposed DDFS architecture. The hardware code in Verilog runs on PC with the ModelSim simulation tool [42] and Xilinx ISE smart compiler [43]. It is noted that the throughput can be improved by using the proposed architecture, while the computation accuracy is the same as that obtained by using the conventional one with the same word length. Thus, the proposed DDFS architecture is able to improve the power consumption and computation speed significantly. Moreover, all the control signals are internally generated on-chip. The proposed DDFS provides both high performance and less hardware.

The chip has been synthesized by using the TSMC 0.18 μm 1P6M CMOS cell libraries [44]. The physical circuit has been synthesized by the Astro tool. The circuit has been evaluated by DRC, LVS, and PVS [45]. Figure 14 shows the cell-based design flow.

Figure 15 shows layout view of the proposed scaling-free CORDIC-based DDFS. The core size obtained by the Synopsys design analyzer is $452 \times 452\,\mu$m^2. The power consumption obtained by the PrimePower is 0.302 mW with clock rate of 500 MHz at 1.8 V. The tuning latency is 11 clock cycles. All of the control signals are internally generated on-chip. The chip provides both high throughput and low gate count.

5. Conclusion

In this paper, we present a novel DDFS architecture-based on the scaling-free CORDIC algorithm with small ROM and pipeline data path. Circuit emulation shows that the proposed high performance architecture has the advantages of high precision, high data rate, and simple hardware. For 16-bit DDFS, the SFDR of the proposed architecture is more than 86.85 dBc. As shown in Table 3, the proposed DDFS is superior to the previous works in terms of SFDR, SNR, output resolution, and tuning latency [6, 17, 18, 26, 27]. According to the high performance of the proposed DDFS, it is very suited for medical instruments and body care network systems [46–49]. The proposed DDFS with the use of the portable Verilog is a reusable IP, which can be implemented in various processes with tradeoffs of performance, area, and power consumption.
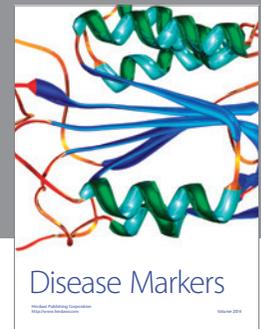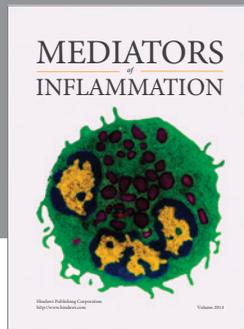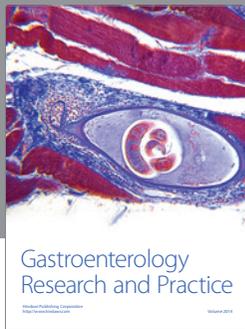
Acknowledgment

References

[1] J. Tierney, C. Rader, and B. Gold, "A digital frequency synthesizer," *IEEE Transactions on Audio and Electroacoustics*, vol. 19, no. 1, pp. 48–57, 1971.

[2] S. Chen, M. Zhao, G. Wu, C. Yao, and J. Zhang, "Recent advances in morphological cell image analysis," *Computational and Mathematical Methods in Medicine*, vol. 2012, Article ID 101536, 10 pages, 2012.

[3] Z. Teng, A. J. Degnan, U. Sadat et al., "Characterization of healing following atherosclerotic carotid plaque rupture in acutely symptomatic patients: an exploratory study using in vivo cardiovascular magnetic resonance," *Journal of Cardiovascular Magnetic Resonance*, vol. 13, article 64, 2011.

[4] S. Chen and X. Li, "Functional magnetic resonance imaging for imaging neural activity in the human brain: the annual progress," *Computational and Mathematical Methods in Medicine*, vol. 2012, Article ID 613465, 9 pages, 2012.

[5] J. Vankka, "Methods of mapping from phase to sine amplitude in direct digital synthesis," in *Proceedings of the 50th IEEE International Frequency Control Symposium*, pp. 942–950, June 1996.

[6] S. C. Yi, K. T. Lee, J. J. Chen, and C. H. Lin, "A low-power efficient direct digital frequency synthesizer based on new two-level lookup table," in *Proceedings of the Canadian Conference on Electrical and Computer Engineering (CCECE '06)*, pp. 963–966, May 2006.

[7] D. A. Sunderland, R. A. Strauch, S. S. Wharfield, H. T. Peterson, and C. R. Cole, "CMOS/SOS frequency synthesizer LSI circuit for spread spectrum communications," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 4, pp. 497–506, 1984.

[8] H. T. Nicholas, H. Samueli, and B. Kim, "Optimization of direct digital frequency synthesizer performance in the presence of finite word length effects," in *Proceedings of the 42nd Annual Frequency Control Symposium*, pp. 357–363, June 1988.

[9] L. A. Weaver and R. J. Kerr, "High resolution phase to sine amplitude conversion," U.S. Patent 4 905 177, 1990.

[10] A. Bonfanti, D. De Caro, A. D. Grasso, S. Pennisi, C. Samori, and A. G. M. Strollo, "A 2.5-GHz DDFS-PLL with 1.8-MHz bandwidth in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1403–1413, 2008.

[11] A. Bellaouar, M. S. O'brecht, A. M. Fahim, and M. I. Elmasry, "Low-power direct digital frequency synthesis for wireless communications," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 385–390, 2000.

[12] A. Bellaouar, M. S. O'Brecht, and M. I. Elmasry, "Low-power direct digital frequency synthesizer architecture," U.S. Patent 5 999 581, 1999.

[13] M. M. El Said and M. I. Elmasry, "An improved ROM compression technique for direct digital frequency synthesizers," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 437–440, May 2002.

[14] G. C. Gielis, R. van de Plassche, and J. van Valburg, "A 540-MHz 10-b polar-to-Cartesian converter," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 11, pp. 1645–1650, 1991.

[15] D. De Caro, E. Napoli, and A. G. M. Strollo, "Direct digital frequency synthesizers with polynomial hyperfolding technique," *IEEE Transactions on Circuits and Systems II*, vol. 51, no. 7, pp. 337–344, 2004.

[16] Y. H. Chen and Y. A. Chau, "A direct digital frequency synthesizer based on a new form of polynomial approximations," *IEEE Transactions on Consumer Electronics*, vol. 56, no. 2, pp. 436–440, 2010.

[17] H. Jafari, A. Ayatollahi, and S. Mirzakuchaki, "A low power, high SFDR, ROM-less direct digital frequency synthesizer," in *Proceedings of the IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC '05)*, pp. 829–832, December 2005.

[18] A. Ashrafi and R. Adhami, "Theoretical upperbound of the spurious-free dynamic range in direct digital frequency synthesizers realized by polynomial interpolation methods," *IEEE*

Transactions on Circuits and Systems I, vol. 54, no. 10, pp. 2252–2261, 2007.

[19] S. Nahm, K. Han, and W. Sung, "CORDIC-based digital quadrature mixer: comparison with a ROM-based architecture," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '98)*, pp. 385–388, June 1998.

[20] A. Madisetti, A. Y. Kwentus, and A. N. Willson, "100-MHz, 16-b, direct digital frequency synthesizer with a 100-dBc spurious-free dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 8, pp. 1034–1043, 1999.

[21] A. Madisetti and A. Y. Kwentus, "Method and apparatus for direct digital frequency synthesizer," U.S. Patent 5 737 253, 1998.

[22] E. Grayver and B. Daneshrad, "Direct digital frequency synthesis using a modified CORDIC," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '98)*, vol. 5, pp. 241–244, June 1998.

[23] C. Y. Kang and E. E. Swartzlander Jr., "Digit-pipelined direct digital frequency synthesis based on differential CORDIC," *IEEE Transactions on Circuits and Systems I*, vol. 53, no. 5, pp. 1035–1044, 2006.

[24] T. Y. Sung and H. C. Hsin, "Design and simulation of reusable IP CORDIC core for special-purpose processors," *IET Computers and Digital Techniques*, vol. 1, no. 5, pp. 581–589, 2007.

[25] T. Y. Sung, L. T. Ko, and H. C. Hsin, "Low-power and high-SFDR direct digital frequency synthesizer based on hybrid CORDIC algorithm," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '09)*, pp. 249–252, May 2009.

[26] S. Sharma, P. N. Ravichandran, S. Kulkarni, M. Vanitha, and P. Lakshminarsimahan, "Implementation of Para-CORDIC algorithm and it's applications in satellite communication," in *Proceedings of the International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom '09)*, pp. 266–270, October 2009.

[27] D. De Caro, N. Petra, and A. G. M. Strollo, "Digital synthesizer/mixer with hybrid CORDIC—multiplier architecture: error analysis and optimization," *IEEE Transactions on Circuits and Systems I*, vol. 56, no. 2, pp. 364–373, 2009.

[28] J. Volder, "The CORDIC trigonometric computing technique," *IRE Transactions on Electronic Computers*, vol. 8, no. 3, pp. 330–334, 1959.

[29] J. S. Walther, "A unified algorithm for elementary functions," in *Proceedings of the Joint Computer Conference*, pp. 379–385, 1971.

[30] S. Chen, W. Huang, C. Cattani, and G. Altieri, "Traffic dynamics on complex networks: a survey," *Mathematical Problems in Engineering*, vol. 2012, Article ID 732698, 23 pages, 2012.

[31] W. Huang and S. Y. Chen, "Epidemic metapopulation model with traffic routing in scale-free networks," *Journal of Statistical Mechanics*, vol. 2011, no. 12, Article ID P12004, 19 pages, 2011.

[32] H. Shi, W. Wang, N. M. Kwok, and S. Y. Chen, "Game theory for wireless sensor networks: a survey," *Sensors*, vol. 12, no. 7, pp. 9055–9097, 2012.

[33] C. Cattani, S. Y. Chen, and G. Aldashev, "Information and modeling in complexity," *Mathematical Problems in Engineering*, vol. 2012, Article ID 868413, 4 pages, 2012.

[34] Y. H. Hu, "CORDIC-based VLSI architectures for digital signal processing," *IEEE Signal Processing Magazine*, vol. 9, no. 3, pp. 16–35, 1992.

[35] K. Maharatna, A. S. Dhar, and S. Banerjee, "A VLSI array architecture for realization of DFT, DHT, DCT and DST," *Signal Processing*, vol. 81, no. 9, pp. 1813–1822, 2001.

[36] T. Y. Sung, "Memory-efficient and high-speed split-radix FFT/IFFT processor based on pipelined CORDIC rotations," *IEE Proceedings*, vol. 153, no. 4, pp. 405–410, 2006.

[37] C. Cattani, "On the existence of wavelet symmetries in archaea DNA," *Computational and Mathematical Methods in Medicine*, vol. 2012, Article ID 673934, 16 pages, 2012.

[38] M. Li, "Approximating ideal filters by systems of fractional order," *Computational and Mathematical Methods in Medicine*, vol. 2012, Article ID 365054, 6 pages, 2012.

[39] S. Chen, Y. Zheng, C. Cattani, and W. Wang, "Modeling of biological intelligence for SCM system optimization," *Computational and Mathematical Methods in Medicine*, vol. 2012, Article ID 769702, 30 pages, 2012.

[40] C. Cattani, "Harmonic wavelet approximation of random, fractal and high frequency signals," *Telecommunication Systems*, vol. 2009, pp. 207–217, 2009.

[41] SMIMS Technology Corp., 2010, http://www.smims.com/.

[42] ModelSim—Simulation and debug, 2010, http://model.com/content/modelsim-pe-simulation-and-debug.

[43] Xilinx FPGA products, 2010, http://www.xilinx.com/products/.

[44] Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu City, Taiwan, and National Chip Implementation Center (CIC), National Science Council, Hsinchu City, Taiwan, TSMC 0.18 CMOS Design Libraries and Technical Data, v.1.6, 2010.

[45] Cadence Design Systems, 2010, http://www.cadence.com/products/pages/default.aspx.

[46] D. Prutchi and M. Norris, *Design and Development of Medical Electronic Instrumentation: A Practical Perspective of the Design, Construction, and Test of Medical Devices*, John Wiley & Sons, 2005.

[47] N. Li, J. Guo, H. S. Nie, W. Yi, H. J. Liu, and H. Xu, "Design of embedded bio-impedance analyzer based on digital auto balancing bridge method," *Applied Mechanics and Materials*, vol. 136, pp. 396–401, 2011.

[48] K. H. Lin, W. H. Chiu, and J. D. Tseng, "Low-complexity architecture of carrier frequency offset estimation and compensation for body area network systems," *Computer and Mathematics with Applications*, vol. 64, no. 5, pp. 1400–1408, 2012.

[49] J. Guo and P. Dong, "Design of dual phase signals generator based on AD9833," *Lecture in Electrical Engineering*, vol. 139, pp. 7–13, 2012.

The Scientific
World Journal

Gastroenterology
Research and Practice

MEDIATORS
of
INFLAMMATION

Journal of
Diabetes Research

Disease Markers

Journal of
Immunology Research

International Journal of
Endocrinology

PPAR Research

BioMed
Research International

Hindawi

Submit your manuscripts at
http://www.hindawi.com

Journal of
Ophthalmology

Stem Cells
International

ᵉCAM

Evidence-Based
Complementary and
Alternative Medicine

Journal of
Obesity

Journal of
Oncology

Computational and
Mathematical Methods
in Medicine

Behavioural
Neurology

Parkinson's
Disease

AIDS
Research and Treatment

Oxidative Medicine and
Cellular Longevity